

R09

Code No: D5707

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech II - Semester Examinations, March/April 2011

VLSI SIGNAL PROCESSING

(VLSI SYSTEM DESIGN)

Time: 3hours

Max. Marks: 60

**Answer any five questions
All questions carry equal marks**

1. Explain a 3 tap FIR filter using:
a) Block diagrams.
b) Signal flow graphs.
c) Data flow graphs. [4+4+4]
2. Explain pipelining & parallel processing for low power with examples. [12]
3. Explain register minimization using folded architectures for the following:
a) Bi Quad filter.
b) IIR filters. [6+6]
4. Explain applications of unfolding. [12]
5. Explain FIR systolic arrays design. [12]
6. Construct a 2×3 convolution algorithm using modified wino-grad algorithm with $m(p)=p(p-1)(p+1)$. [12]
7. Explain power estimation approaches. [12]
8. Explain processors for multimedia signal processing. [12]
